(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 069 495 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
17.01.2001 Bulletin 2001/03

(51) Int Cl.[7]: **G06F 1/32**

(21) Application number: **00305907.8**

(22) Date of filing: **12.07.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **14.07.1999 US 353684**

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(54) Power management fault strategy for automotive multimedia system

(57) A multimedia/personal computer-based system for operating information, communication, and entertainment devices in a mobile vehicle uses a power management strategy which reduces power consumption and boot-up time in a manner which facilitates use of a complex instruction set computing (CISC) processor system. A power management fault strategy detects fault conditions and restores proper operation without user intervention. A low power microprocessor (25)off-board of the main motherboard (10) switches a plurality of regulated voltages to the main motherboard (10) and other devices. The main application microprocessor (13) on the main motherboard (10) sends periodic status messages to the low power microprocessor(25). If a time limit between successive status messages is exceeded, then the low power microprocessor (25) takes corrective action such as sending messages to the main application microprocessor (13), sending a reset signal to the main application microprocessor, or removing or cycling the regulated voltages being provided to the main motherboard.

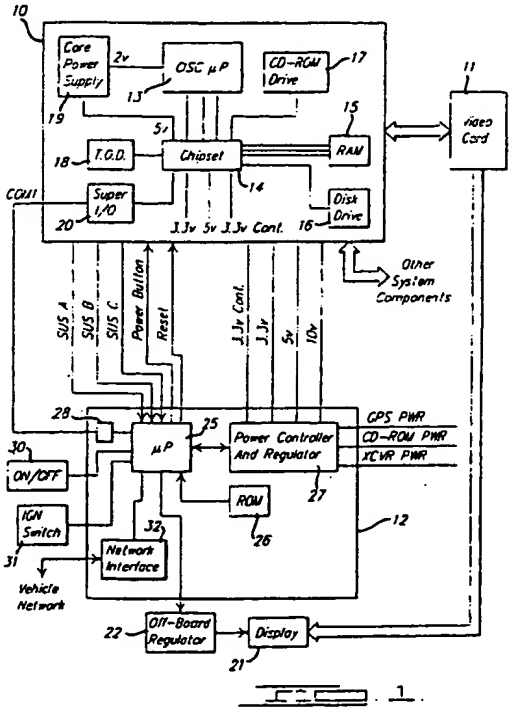

Fig. 1

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media system employing the power management strategy of the present invention.

[0011] Figure 2 is a state diagram showing state transitions of the system in Figure 1.

[0012] Figure 3 is a state diagram showing monitoring of heartbeat messages during full-power operation.

[0013] Figure 4 is a state diagram showing fault management during wake-up of the main application microprocessor.

[0014] Figure 5 is a state diagram showing fault management during shutdown to the suspend-to-RAM state of the main application microprocessor, and;

[0015] Figure 6 is a state diagram showing fault management during shutdown to the suspend-to-disk state of the main application microprocessor.

[0016] Referring to Figure 1, a motherboard 10 is connected to a video processor card 11 and a vehicle input/output processor (VIOP) board 12. Motherboard 10 includes a complex instruction set computing (CISC) processor 13 which may comprised of an Intel Celleron processor, for example. A support chip set 14 is connected to processor 13 and is adapted to function specifically with microprocessor 13. Support chip set 14 may be one or more integrated circuits and may preferably be comprised of north and south portions of an Intel Banister Bridge.

[0017] Chip set 14 provides interfaces between processor 13 and various other devices and provides local power conditioning and management for processor 13. Support chip set 14 includes a DRAM memory controller for controlling a DRAM memory 15. Chip set 14 also includes interface controllers for a mass storage devices such as a disk drive 16 and a CD-ROM drive 17. Processor 13 is a main application processor and executes operating system software and application programs contained on disk drive 16 and/or CD-ROM drive 17.

[0018] A time of day (TOD) unit 18 is connected to chip set 14 and keeps track of time of day in a conventional manner. A small on-board battery (not shown) is preferably provided to maintain operation of TOD unit 18 even when power is off to motherboard 10.

[0019] Chip set 14 receives several different regulated voltages from VIOP 12 as is described below. Chip set 14 uses the regulated voltages to provide power to processor 13 and DRAM 15 according to its own, conventional power management strategy. Motherboard 10 may further include a core power supply 19 driven by chip set 14 to provide a regulated voltage at a value not being supplied by VIOP 12.

[0020] A super-input/output (I/O) interface 20 is connected to chip set 14 and provides a serial communications port COM1 which is connected to VIOP 12. The serial communications link carries messages between processor 13 and VIOP 12 relating to power management and to input and output data and control signals.

[0021] Motherboard 10 includes other conventional components which are not shown such as a BIOS unit and standard bus interfaces such as ISA, PCI, and USB interfaces. Video card 11 may be connected to a PCI expansion slot, for example. Video card 11 includes a video output connected to a display 21 which is powered by an off-board regulator 22 under control of VIOP 12.

[0022] VIOP 12 includes a reduced power microprocessor 25 which executes program instructions contained in a read-only memory (ROM) 26, for example. Reduced power microprocessor 25 may be comprised of a Motorola 68 HC 912 processor, for example, or other low power processor of the type often used on automotive applications. A principle job of processor 25 is to control a power controller and regulator 27 which has a plurality of switched and unswitched regulated voltage outputs. For example, switched outputs of 3.3V, 5V, and 10V are provided along with an unswitched (i.e., continuous) supply of 3.3V. Each of these regulated voltages is provided to main motherboard 10 and then distributed to various components which use them, including chip set 14. These voltages are used to operate microprocessor 13, power memory 15 for refreshing and accessing memory contents, and for powering portions of chip set 14 itself. In addition, power may be directly supplied to disk drive 16, CD-ROM 17 and TOD unit 18.

[0023] Power controller and regulator 27 may also provide regulated voltages to devices located remotely from motherboard 10 and VIOP 12. For example, a separate, remote module may include a GPS receiver and a wireless data transceiver receiving GPS power (GPS PWR) and transceiver power (XCVR PWR) from power controller and regulator 27.

[0024] VIOP 12 includes a physical interface 28 for providing a serial port connection for microprocessor 25 to communicate with the COM1 port of motherboard 10. In addition, there are several direct communication lines connected between motherboard 10 and microprocessor 25. Microprocessor 25 provides a power button signal in response to an on/off switch 30 controlled by the user to indicate when to place the multimedia system in an in-use condition, and a reset signal for causing the main application processor 13 to reboot. Chip set 14 provides three distinct signals SUS A, SUS B, and SUS C, which identify the suspended power state in which the power management strategy of chip set 14 is operating.

[0025] Microprocessor 25 also receives a signal from an ignition switch 31 to identify whether the vehicle is in a powered state or an unpowered state. Based upon the state of ignition switch 31 and on/off switch 30, microprocessor 25 and microprocessor 13 each determine an appropriate power state for main application processor 13 and chip set 14. Depending upon the current state and next desired state of microprocessor 13 and chip set 14, microprocessor 25 may merely verify that the correct state has been implemented by chip set 14, it may command a different state over the serial communication link, or it may switch the state of power controller and regulator 27 to provide different regulated voltages to main motherboard 10. Also based upon the

pend-to-RAM state draws between 70 and 100 mA of current and the state may be exited by pressing the power button while the ignition is on, or by a reset signal from the VIOP.

[0034] In the suspend-to-disk (D3) power state, an image or snapshot of the DRAM memory contents is stored to disk (preferably a compact flash drive). The north bridge of the chip set is powered down and the south bridge is mostly powered down except for the south bridge section that has power control. Current draw is between 1 and 2 mA in this power state. Current draw results in part from the need to drive the SUS A, B, and C lines for giving the power state status of the main controller and chip set.

[0035] The serial communications link between microprocessors 13 and 25 carries various types of messages, such as input/output data and control signals for various peripheral devices. In addition, fault management and status messages are communicated to permit reduced power microprocessor 25 to ensure proper operation of the multimedia system. Thus, if the main application microprocessor becomes "locked-up" or "frozen," this is detected by the reduced power microprocessor and action can be taken to restore proper operation without requiring user intervention. Furthermore, if the main application microprocessor assumes a power state other than the one required by the power management strategy, this is detected and, if not correctable, then the reduced power microprocessor avoids possible excessive current consumption by shutting off most power to the main application microprocessor.

[0036] The fault management strategy of the present invention employs a status message (or "heartbeat" message) that is programmed to be sent periodically by the main application microprocessor to the reduced power microprocessor whenever the main application microprocessor is running (i.e., operating in the Full Power state or the Standby+ state). When the processor is first booted up, there will be some delay before it is able to send its first heartbeat message. Thereafter, the main application processor is programmed to generate a regular heartbeat message (e.g., every 5 seconds). If the reduced power microprocessor fails to receive an expected heartbeat message within this predetermined time, then the main application processor is assumed to have malfunctioned and corrective action is taken.

[0037] This portion of the fault strategy is shown in greater detail in Figure 3. After initiation of a boot-up of the main application processor, the fault strategy enters a state 50 wherein a waiting period is established within the reduced power microprocessor of 60 seconds. During this 60 second time period, a heartbeat message would be expected from the main application processor if boot-up to a normal running state is achieved. If, as expected, a heartbeat message is received during the 60 second time period, then a shorter waiting period of 5 seconds is established in a state 51. If a heartbeat message is received during the shorter waiting period, then the fault strategy stays in state 51 with a re-initiation of the 5 second waiting period. If a heartbeat message is not detected by the reduced power microprocessor during the 5 second waiting period, then it enters state 52 and sends a reset signal to the main application processor to re-boot it. Then the reduced power microprocessor returns to state 50 to establish the 60 second waiting period.

[0038] If a heartbeat message is not received during the 60 second time period in state 50, then a series of resets followed by additional 60 second waiting periods are established in states 53 through 58. If a heartbeat message is received while in states 54, 56, or 58, then normal operation results in state 51. If on the final try in state 58 no heartbeat message is received, then the regulated voltages supplied to the main motherboard by the VIOP power controller and regulator are cycled off and then back on in an attempt to recover proper operation of the main application microprocessor. Then the main application microprocessor attempts to restart or reboot, and the fault strategy returns to state 50.

[0039] A portion of the fault strategy of the present invention active during an attempt to wake up the main application processor from a suspend-to-disk (OFF or D3) condition or a suspend-to-RAM (SUSPEND or S3) condition is shown in Figure 4. The main application microprocessor is in SUSPEND or OFF initially in state 60. A transition to state 61 is made in response to a wake-up command. Such a wake-up command may be a signal generated by any devices in the system such as a user control push button (e.g., power button), the vehicle ignition switch, or insertion of a media (e.g., CD-ROM, CD audio, or cassette tape). The main motherboard may respond directly to these signals and may generate a wake-up command itself. In addition, the reduced power microprocessor monitors these conditions and determines when existing conditions should wake the main application processor to its full-powered operating state. Then, in state 61, it checks status lines SUS A, B, and C, to determine the power state of the main application processor. If these lines indicate a run state, then no further action is taken. However, if these lines indicate an OFF or SUSPEND state, then the reduced power microprocessor transmits its own wake-up command over the serial communication link in state 62. The wake-up command is retried up to 2 more times (after sufficient waiting periods) if the command is unsuccessful. After the final try, then the state of the vehicle ignition is determined. If the ignition is off, then there should be no further consumption of current and the regulated voltages are turned off in state 63. On the other hand, if the ignition is on then the regulated voltages are cycled off and back on in state 64 in an attempt to restore proper system operation. Then another wake-up command is transmitted and a return is made to state 61.

[0040] A portion of the fault strategy of the present invention active during an attempt to shutdown the main application processor to a suspend-to-RAM (SUSPEND

sending a reset signal from said reduced power microprocessor (25) to said main application microprocessor (13) if said status message is not received during said predetermined time period.

2. A method as claimed in claim 1, further comprising the steps of:

establishing a further predetermined time period in said reduced power microprocessor after sending said reset signal during which a status message is expected to be received from said main application microprocessor;
cycling said regulated voltages off and then back on to said main application microprocessor if said status message is not received during said further predetermined time period; and
restarting said main application microprocessor.

3. A method as claimed in claim 1, wherein, when said main application microprocessor is not in a full-powered operating state, said reduced power microprocessor monitors conditions which should wake said main application microprocessor into said full-powered operating state, and wherein said method further comprises the steps of:

said reduced power microprocessor determining whether said main application microprocessor has correctly assumed said full-powered operating state;
sending a wake-up message from said reduced power microprocessor to said main application microprocessor when it has not correctly assumed said full-powered operating state;
resending said wake-up message from said reduced power microprocessor to said main application microprocessor if it again fails to assume said full-powered operating state;
cycling said regulated voltages off and then back on to said main application microprocessor if it again fails to assume said full-powered operating state; and
resending said wake-up message from said reduced power microprocessor to said main application microprocessor.

4. A method as claimed in claim 1, wherein, when said main application microprocessor is in a full-powered operating state, said reduced power microprocessor monitors conditions which should shut down said main application microprocessor into a suspended operating state, and wherein said method further comprises the steps of:

said reduced power microprocessor determining whether said main application microprocessor has correctly assumed said suspended operating state;
sending a shutdown message from said reduced power microprocessor to said main application microprocessor when it has not correctly assumed said suspended operating state;
resending said shutdown message from said reduced power microprocessor to said main application microprocessor if it again fails to assume said suspended operating state;
sending a reset signal from said reduced power microprocessor to said main application microprocessor if it again fails to assume said suspended operating state; and
resending said shutdown message from said reduced power microprocessor to said main application microprocessor.

5. A method as claimed in claim 4, further comprising the step of:

turning off said regulated voltages if said main application microprocessor again fails to assume said suspended operating state.

6. A method as claimed in claim 1, wherein, when said main application microprocessor is in a suspend-to-RAM operating state, said reduced power microprocessor measures an extended time period after which said main application microprocessor should perform a suspend-to-disk operation, and wherein said method further comprises the steps of:

said reduced power microprocessor determining whether said main application microprocessor has correctly assumed a suspend-to-disk operating state;
sending a wake-up message from said reduced power microprocessor to said main application microprocessor when it has not correctly assumed said suspend-to-disk operating state;
sending a suspend-to-disk message from said reduced power microprocessor to said main application microprocessor;
resending said suspend-to-disk message from said reduced power microprocessor to said main application microprocessor if it fails to assume said suspend-to-disk operating state;
sending a reset signal from said reduced power microprocessor to said main application microprocessor if it again fails to assume said suspend-to-disk operating state;
sending a suspend-to-disk message from said reduced power microprocessor to said main application microprocessor; and
turning off said regulated voltages if said main application microprocessor again fails to as-

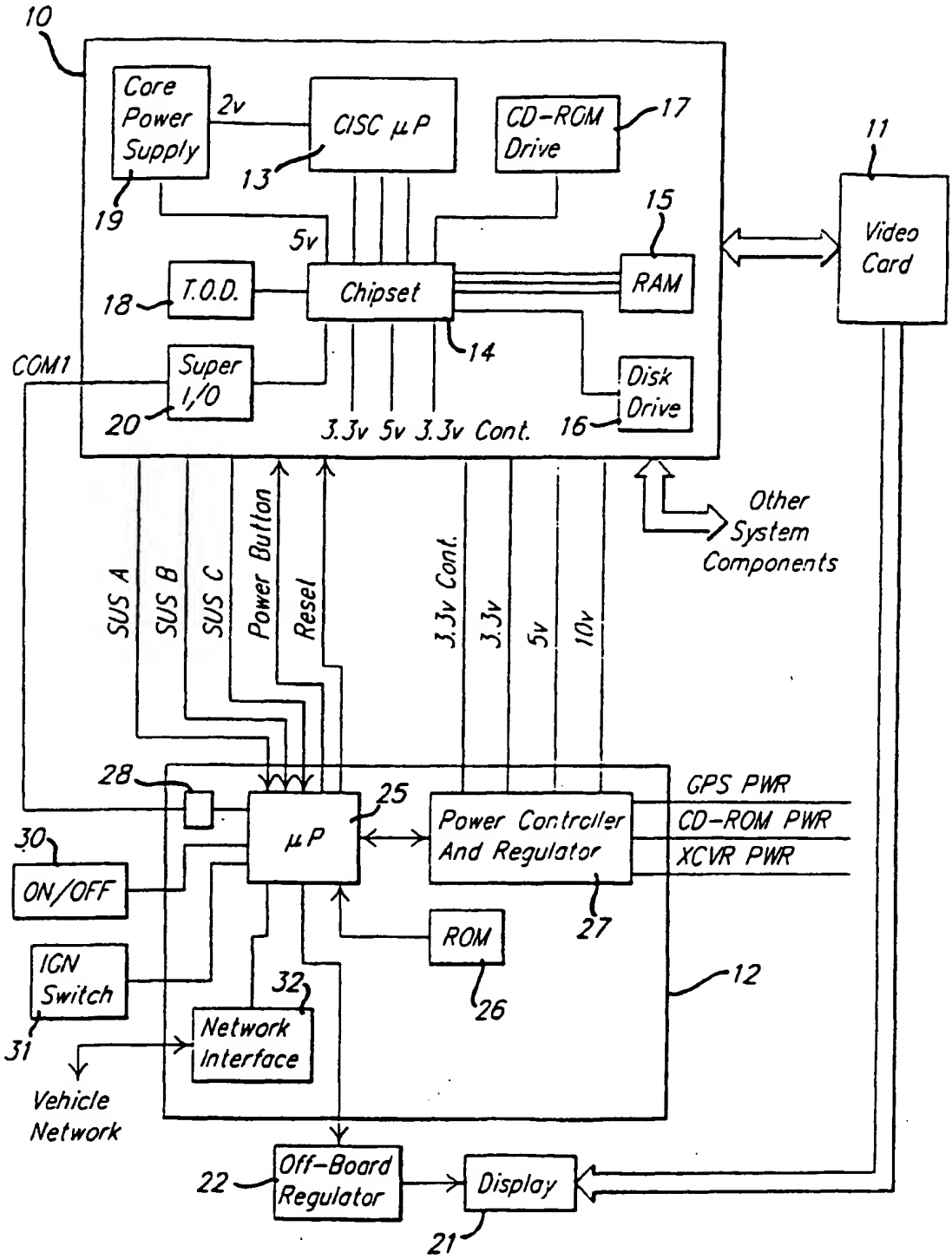
10
Core Power Supply
2v
CISC µP
13
CD-ROM Drive
17
11
19
5v
15
Video Card
18
T.O.D.
Chipset
RAM
14
COM1
Super I/O
20
3.3v 5v 3.3v Cont.
16
Disk Drive
Other System Components
SUS A
SUS B
SUS C
Power Button
Resel
3.3v Cont.
3.3v
5v
10v
28
25
GPS PWR
µP
Power Controller And Regulator
CD-ROM PWR
XCVR PWR
30
ON/OFF
27
ROM
IGN Switch
12
32
26
Network Interface
31
Vehicle Network
22
Off-Board Regulator
Display
21

FIG. 1

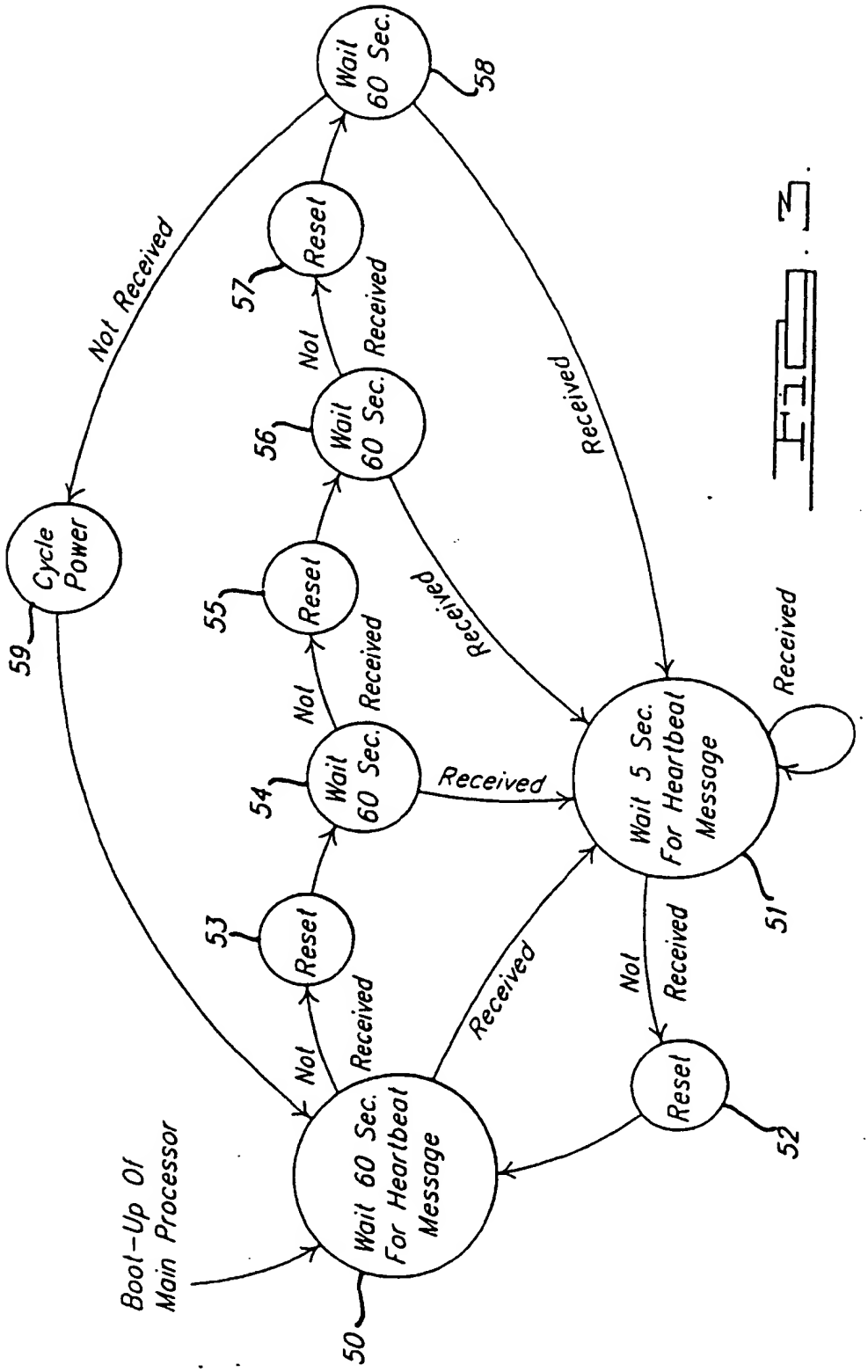
Boot-Up Of Main Processor
Wait 60 Sec. For Heartbeat Message
50
Reset
52
Wait 5 Sec. For Heartbeat Message
51
Reset
53
Wait 60 Sec.
54
Reset
55
Wait 60 Sec.
56
Reset
57
Wait 60 Sec.
58
Cycle Power
59
Not Received
Received
Not
Received
Received
Not
Received
Received
Not
Received
Received
Received
Received

Fig. 3

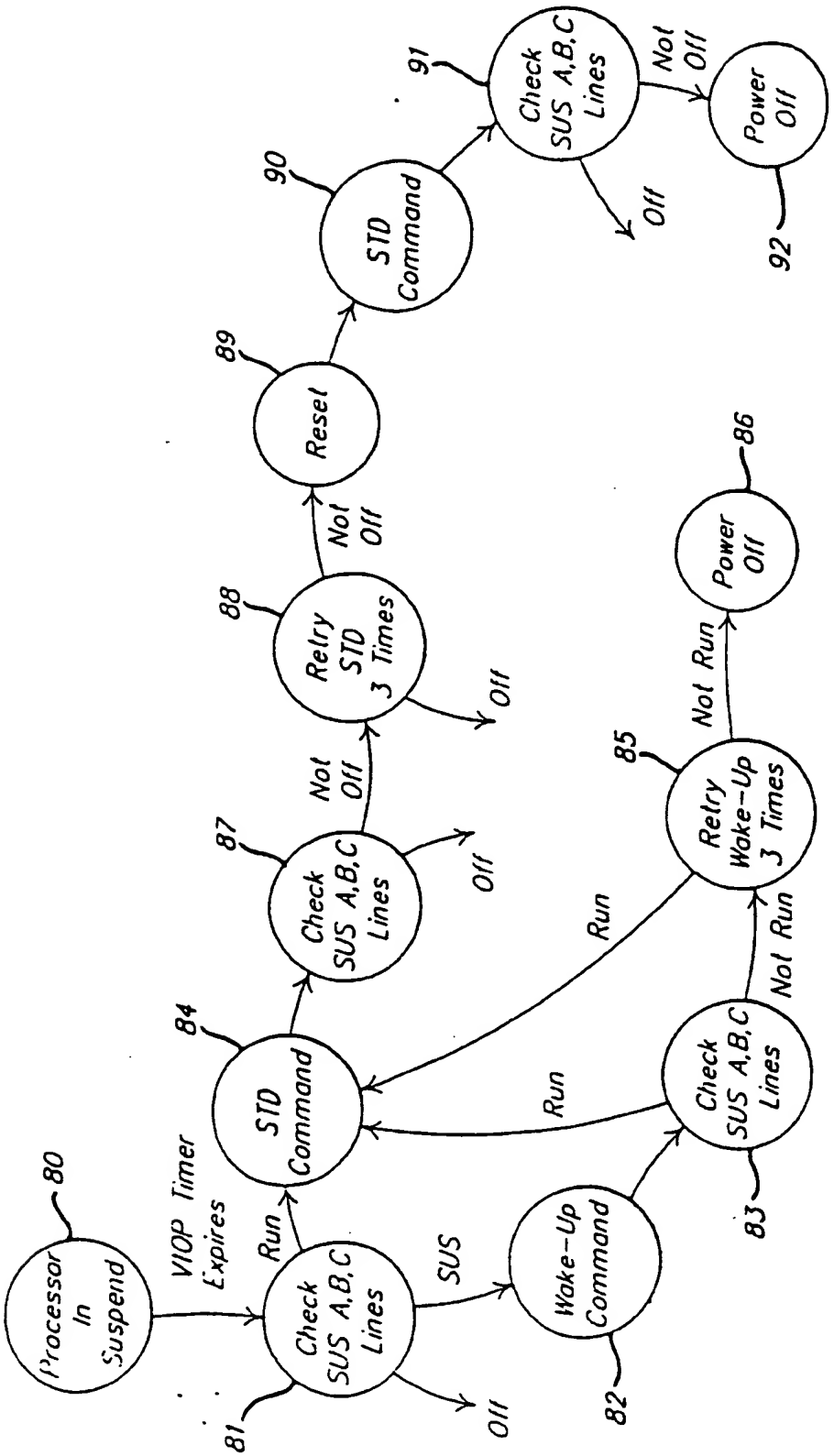
Processor In Suspend
80
VIOP Timer Expires
Run
Check SUS A,B,C Lines
81
Off
SUS
Wake-Up Command
82
Check SUS A,B,C Lines
83
Not Run
Run
STD Command
84
Run
Check SUS A,B,C Lines
87
Off
Not Off
Retry STD 3 Times
88
Off
Not Off
Reset
89
STD Command
90
Check SUS A,B,C Lines
91
Off
Not Off
Power Off
92
Retry Wake-Up 3 Times
85
Not Run
Power Off
86

FIG. 6